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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/972,855	SUGIZAKI, YOSHIAKI	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspond nce address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,12,13 and 19-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3, 12, 13 and 19-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required.

Claims 3 and 20 recite "...wherein the average density of arrangement such thusly arranged connecting terminals ..." . The specification does not describe an explicit aspect of the average density of arrangement such thusly arranged connecting terminals. Note that the specification does not disclose any density of the arrangement of the connecting terminals especially about the connecting terminals such thusly arranged.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3, 12, 13, 19 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 3 and 20 recite "...wherein the average density of arrangement such thusly arranged connecting terminals ..." which does not carry a clear meaning. Especially the limitation of "the average density of arrangement such thusly arranged connecting terminals" implies that there is an actual density of the arrangement of such thusly arranged the connecting terminals.

Claims 12, 13 and 19 are dependent on the rejected base claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 12, 13, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakui et al. (U.S. Pat. No. 6,239,495) in view of Iijima et al. (U.S. Pat. No. 5,729,435).

Regarding claim 3, Sakui et al. show in Fig. 1 a semiconductor device comprising;

a first semiconductor chip (1-2) where a semiconductor element (3; a multiple wiring layer) is formed;

a plurality of first connecting terminals (8) arranged on a semiconductor element formation surface side in the first semiconductor chip (1-2) and connected electrically to the semiconductor element (3);

conductive members (4) buried in a plurality of through holes (5) that go through the first semiconductor (1-2) coupled to the second 1-1 to n-th semiconductor chips (12-4 in Fig. 3);

second connecting terminals on the back of the first chip are (shown at 8-1, 8-2, ... in Fig.3); and

the average density of arrangement of the one of the first connecting terminals and the second connecting terminals is lower than another of the first connecting terminals and the second connecting terminals as shown in Fig. 3. In detail, Fig.3 shows that the number of the

second connecting terminals (7 metal bumps; 8-1 through 8-7) is more than that of the first connecting terminals (five metal bumps) which are formed on the first surface of the chip 12-1.

The chips are mounted on an assembly board (col. 5, lines 25-33 and col. 1 lines 62-63), therefore it is obvious that at least either the first connecting terminals or the second connecting terminals is coupled to an assembly board to have a proper electrical operation in devices.

Also see the respective portions of the specification such as col. 4, lines 60-66.

Sakui et al. do not explicitly show that one of the connecting terminals is facing to the assembly board. Iijima et al. show in Fig. 17 a flip-chip arrangement which conductive bumps 206 is facing the board 202. Also see Fig. 4 for a flip chip configuration. . It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Iijima et al. to the device of Sakui et al. to have a flip chip arrangement since a flip chip configuration provides a higher density and a better performance for a device circuit.

Regarding claim 12, Sakui et al. show in Fig. 1, the semiconductor further comprising a second semiconductor chip 1-1 stacked on the first semiconductor chip 1-2, wherein at least portion of the connecting terminals 8 arranged on a stacked surface between the first semiconductor chip 1-2 and the second semiconductor chip of the first connecting terminals and the second connecting terminals in the first semiconductor chip is coupled to the second semiconductor chip (col. 4, line 58- col. 5, line 12).

Regarding claim 13, Sakui et al. show in Fig. 3, the semiconductor further comprising a second to an n-th (wherein n is a positive integer of three or more) semiconductor chips stacked above first semiconductor chip, wherein at least portion of the connecting terminals arranged on a stacked surface between the first semiconductor chip and the second semiconductor chip of the

first connecting terminals and the second connecting terminals in the first semiconductor chip is coupled to the second to n-th semiconductor chip.

Regarding the specific connections between the chips, see the respective portions of the specification, for example, from col. 5, line 30 to col. 6, line 9.

Regarding claim 19, Sakui et al. show in Fig. 1 and Fig.3, the semiconductor wherein said at least portion of the plurality of connecting terminals comprising conductive bumps 8's.

Claims 3, 12, 13, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakui et al. in view of Komiyama (U.S. Pat. No. 6,424,050)

Regarding claim 3, Sakui et al. show in Fig. 1 a semiconductor device comprising;

a first semiconductor chip 1-2 where a semiconductor element 3 is formed;

a plurality of first connecting terminals 8 arranged on a semiconductor element formation surface side in the first semiconductor chip 1-2, and connected electrically to the semiconductor element 3;

conductive members 4 buried in a plurality of through holes 5 that go through the first semiconductor 1-2 coupled to the second 1-1 to n-th semiconductor chips (12-4 in Fig. 3);

second connecting terminals on the back of the first chip are shown at 8-1, 8-2, ... in Fig.3; and

the average density of arrangement of the one of the first connecting terminals and the second connecting terminals is lower than of another of the first connecting terminals and the second connecting terminals as shown in Fig. 3. Fig.3 shows that the number of the second

connecting terminals (7 metal bumps; 8-1 through 8-7) is more than that of the first connecting terminals (5 metal bumps) which are formed on the first surface of the chip 12-1.

Komiyama is further introduced to clearly show the density of the conductive bumps arrangement is different between the first connecting terminals 15 and the second connecting terminals 24, 49 of the first chip 1 in Fig. 4. Also note that the device of Komiyama is a flip chip configuration, therefore at least of the connecting terminals faces the assembly board. It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teaching of Komiyama to have a different numbers of conductive bumps for two connecting terminals in a flip chip configuration in order to have more compact arrangement to reduce a device size.

The chips are mounted on an assembly board (col. 5, lines 25-33 and col. 1 lines 62-63), therefore it is obvious that at least either the first connecting terminals or the second connecting terminals is coupled to an assembly board to have a proper electrical operation in devices.

Also see the respective portions of the specification such as col. 4, lines 60-66.

Subject matters for claims 12, 13 and 19 have been discussed above.

Claims 20 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakui et al. and Iijima et al. as applied to claim 3 above, and further in view of Hsuan et al. (U.S. Pat. No. 6,236,109).

Regarding claims 20 and 25, Sakui et al. show in Figures 1 and 3, a semiconductor device comprising;

a first semiconductor chip 1-2 where a semiconductor element 3 is formed;

a first connecting terminal 8 arranged on a semiconductor element formation 3 surface side in the first semiconductor chip 1-2, and connected electrically to the semiconductor element;

a conductive member 4 buried in a through hole 5 that goes through the first semiconductor chip 1-2;

a second connecting terminal 8-1 arranged on a back surface side of the semiconductor element formation in the first semiconductor chip, and connected electrically to the semiconductor element via the conductive member 4 in 1-2;

a second semiconductor chip 1-1 stacked on the first semiconductor chip 1-2;

a third connecting terminal (a third bump on 12-2) arranged on a semiconductor element formation surface side in the second semiconductor chip12-2;

wherein, one of the first connecting terminal and the second connecting terminal of the semiconductor chip is arranged at a position facing to the third connecting terminal of the second semiconductor chip, the first semiconductor chip and the second semiconductor chip are electrically coupled with each other through the facing connecting terminals (col. 4, line 58 – col. 5, line 12); and

the average density of arrangement of the one of the first connecting terminals and the second connecting terminals is lower than of another of the first connecting terminals and the second connecting terminals as shown in Fig. 3. Fig.3 shows that the numbers of the second connecting terminals (7 metal bumps; 8-1 through 8-7) are more than that of the first connecting terminals (5 metal bumps) which are formed on the first surface of the chip 12-1; and

one of the connecting terminals is facing the assembly board as taught in Iijima et al. and the motivation for combing teachings of Sakui et al. and Iijima et al. has stated above in claim 3.

(Also note that one of the connecting terminals of Hsu faces the assembly board, too.)

either the first connecting terminals of the second connecting terminals is distributed and arranged in the surface area of the semiconductor chip, and power supply (V_{ss}; a ground voltage) is to be applied on a portion of the bumps (bumps 8-1, 8-2, 8-3 of the first chip 12-1 in Fig. 3).

Also note that one of the connecting terminals of Hsu faces the assembly board, too.

The chips are mounted on an assembly board (col. 5, lines 25-33 and col. 1 lines 62-63), therefore it is obvious that at least either the first connecting terminals or the second connecting terminals is coupled to an assembly board.

Also see the respective portions of the specification such as col. 4, lines 60-66.

Sakui et al. and Iijima et al. do not disclose the limitation over the size of the first and second chips.

However, Hsuan et al. show in Fig. 6A a multi-chip packaging device wherein the second semiconductor chip is larger than the first semiconductor chip.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Hsuan et al. to the device of Sakui et al. and Iijima et al. to have a larger second chip connected to a smaller first chip since such an arrangement improves the effect of heat dissipation during installation, thus controlling the chip connection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 21-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakui et al.

Regarding claim 21, Sakui et al. show in Fig. 1 a semiconductor device comprising;

a first semiconductor chip 1-2 where a semiconductor element 3 is formed;

a plurality of first connecting terminals 8 arranged on a semiconductor element formation surface side in the first semiconductor chip 1-2, and connected electrically to the semiconductor element 3;

conductive members 4 buried in a plurality of through holes 5 that go through the first semiconductor 1-2 coupled to the second 1-1 to n-th semiconductor chips (12-4 in Fig. 3);

second connecting terminals on the back of the first chip are shown at 8-1, 8-2, ... in Fig.3; and connected electrically to the semiconductor element via the conductive members,

wherein at least one of the connecting terminals is coupled to an assembly board as discussed in claim 3 above, and

either the first connecting terminals of the second connecting terminals is distributed and arranged in the surface of the semiconductor chip, and power supply (V_{ss}; a ground voltage) is to be applied on a portions of the bumps (bumps 8-1, 8-2, 8-3 of the first chip 12-1 in Fig. 3),.

Limitations regarding claims 22-24 have been discussed in claims 12-13 and 19 accordingly.

Response to Arguments

Applicant's arguments filed on October 29, 2003 have been fully considered but they are not persuasive.

Applicant's response against claims 3, 12, 13 and 19 are not deemed to be persuasive because the combination of Sakui et al. and Iijima et al. (or Sakui et al. and Komiyama) discloses a structure shown in Figure 24 (Applicant's election) of the instant application which claims 3, 12, 13 and 19 are appeared to read on.

Applicant's argument against claim 21 is fully considered but is not deemed to be persuasive. Refer to the rejection of claim 21 for a complete explanation.

Lastly, Applicant's numerous allegation that the examiner relying on basic knowledge or common sense is rather baseless. All the art rejections are based on the disclosures and teachings of references.

If the Applicant wishes to pursue a further contention using such arguments, he is requested to specifically point out how or why the art rejection is not considered and merely based on basic knowledge or common sense.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (703) 305-3998. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (703) 308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmi
November 29, 2003

SUPERVISORY PATENT EXAMINER